REMARKS

The Official Action mailed February 14, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for Two Month Extension of Time* which extends the shortened statutory period for response to July 14, 2002. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the partial consideration of the Information Disclosure Statements filed on July 30, 2001 and October 17, 2001. Applicant understands that foreign references not indicated as considered will be considered when the parent application file is readily available. For the Examiner's convenience, Applicant submits herewith copies of foreign references cited in the above noted Information Disclosure Statements for consideration by the Examiner. It is respectfully requested that the Examiner evidence consideration of these references by providing a copy of the initialed Form PTO-1449 with the next Official Action.

Claims 1-19 were pending in the present application. Claims 1, 7 and 13 have been canceled, claims 1-6, 8-12 and 14-19 have been amended, and new claims 20-42 have been added to recite additional protection to which Applicant is entitled. Claims 2-6, 8-12, and 14-42 are now pending in the present application, of which claims 3, 7, 9, 13, 15, 20, 25, 29, 35 and 40 are independent. For the reasons set forth in detail below, these claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action objects to claims 3, 9 and 15 due to minor informalities. Specifically the exponent "-12" was not in superscript. In response, claims 3, 9 and 15 have been amended to correct this informality. Reconsideration is requested.

Paragraph 4 of the Official Action rejects claims 1-19 under 35 U.S.C. 112, second paragraph. In Paragraph 5, the Official Action questions whether the insulating film including boro-phosphosilicate glass in claims 4, 10 and 16 is formed on the substrate recited in claims 1, 7 and 13. In response, claims 4, 10 and 16 have been amended to clarify the location of the insulating film and now recite that the insulating film including boro-phosphosilicate glass is formed over the thin film transistors. Reconsideration is requested in view of these clarifying amendments.

In paragraph 6 of the Official Action, the term "transmission gate" is questioned. It is respectfully submitted that this term would be readily understood by one of ordinary skill in the art. To this end, Applicant submits herewith two documents that explain the term "transmission gate." These documents are from the internet and include (1) h*ttp://users.ece.gatech.edu/~rdanse/ECE2030/slides/ECE2030_Chapter02_2pp.pdf*, and (2) *http://www.microlab.ch/courses/cbt/cbt-vlsi/trans_gate1.html*.

Paragraph 9 of the Official Action rejects claims 1-19 as obvious based on U.S. Patent 6,236,064 to Mase et al. Paragraph 10 of the Official Action rejects claims 13-19 as being obvious based on the combination of Mase and U.S. Patent 5,581,092 to Takemura. With respect to the leakage current recited in claim 3, the Official Action asserts this feature would be obtained by the transistors resulting from the process made obvious by the combination of Mase and the known process because implantation is not employed.

As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

It is respectfully submitted that the Official Action has failed to establish a *prima facie* case of obviousness since the prior art references, taken alone or in combination,

fail to teach or suggest all of the claim limitations. The present invention is directed to a method of manufacturing a semiconductor device comprising two p-channel thin film transistors connected in series. Applicant respectfully disagrees that the limitation on the leakage current would have been obvious because of the absence of employing implantation. In the present specification it is described that such conspicuous leakage current resulting from NMOS is an impediment in various applications, especially in applications where dynamic operation is needed. For example, in active matrix arrays of liquid crystals or DRAMs, image information or stored information is lost (See page 6, lines 6-11). Although specifically describing the leakage current of NMOS, leakage current of PMOS is also detrimental to operating active matrix devices when PMOS is used in the pixel portion.

According to the present invention, the OFF current (leakage current) can be suppressed to less than 10^{-12} A when a voltage of the drain region is 1V. Therefore, the claimed invention can avoid the problem of losing image information based on the OFF current. As a result, the p-channel thin film transistor formed through the present method can have a small OFF current.

In addition, Mase includes not only p-channel thin film transistors but also n-channel thin film transistors in a pixel (see Fig. 1), while in the claimed invention it is recited that p-channel thin film transistors are used as switching elements. The leakage current of NMOS is 100 times or more as high as that of PMOS (See page 13, lines 22-23). That is, the PMOS has a leakage current much less than NMOS. Thus, the claimed invention is useful to reduce the leakage current in the pixel. Therefore, it is respectfully submitted that one of skill in the art would not have been motivated to modify the teachings of Mase to achieve the present invention since Mase fails to recognize the problems associated with the use of NMOS as disclosed in the present application and discussed above.

Paragraph 10 of the Official Action rejects claims 1-4, 6,-10, 12-16, and 18 under the judicially created the doctrine of obviousness-type double patent based on claims 1-14 of U.S. Patent 6,326,642. Applicant respectfully requests that this rejection be held in abeyance at this time until an indication of allowable subject matter is made. At that

time, Applicant will fully respond to any remaining double patenting rejections as appropriate.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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Potomac Falls, Virginia 20165
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claims 1, 7 and 13 and amend claims 2-6, 8-12 and 14-19 as follows:

2. (Amended) A method according to claim [1] 3, further comprising [the step of]:

forming a blocking film between the substrate and the semiconductor island,

wherein the substrate is a glass substrate;

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

3. (Amended) A method [according to claim 1,] of manufacturing a semiconductor device comprising at least two p-channel thin film transistors,

each of the two p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than [10-12] 10^{-12} A where a voltage of the drain region is 1V.

4. (Amended) A method according to claim [1] 3, further comprising [the step of]:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

5. (Amended) A method according to claim [1] 3, wherein the semiconductor island is a crystalline semiconductor island.

6. (Amended) A method according to claim [1] 3, wherein each of the source and drain regions comprises boron.

8. (Amended) A method according to claim [7] 9 further comprising [the step of]:

forming a blocking film between the substrate and the semiconductor island,

wherein the substrate is a glass substrate;

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

9. (Amended) A method [according to claim 7,] of manufacturing a display device, said display device comprising:

a pixel portion and a driving circuit portion;

at least two p-channel thin film transistors being formed in the pixel portion;

each of the two p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the two p-channel thin film transistors are connected in series,

wherein an off current from each of the p-channel thin film transistors is less than [10-12] 10^{-12} A where a voltage of the drain region is 1V.

10. (Amended) A method according to claim [7] 9, further comprising [the step of]:

forming an interlayer insulating film including boro-phosphosilicate glass over the two p-channel thin film transistors.

11. (Amended) A method according to claim [7] 9, wherein the semiconductor island is a crystalline semiconductor island.

12. (Amended) A device according to claim [7] 9, wherein each of the source and drain regions comprises boron.

14. (Amended) A method according to claim [13] 15 further comprising [the step of]:

forming a blocking film between the substrate and the semiconductor island,

wherein the substrate is a glass substrate,

wherein the blocking film includes,

a silicon nitride film with a thickness in a range of 5-200 nm formed on the glass substrate, and

a silicon oxide film with a thickness in a range of 20-1000 nm formed on the silicon nitride film.

15. (Amended) A method [according to claim 13,] of manufacturing a semiconductor device, said semiconductor device comprising:

at least a first p-channel thin film transistor and a second p-channel thin film transistor;

a transmission gate including a CMOS circuit, said CMOS circuit including at least an n-channel thin film transistor and a third p-channel thin film transistor;

each of the first, second and third p-channel thin film transistors fabricated through the method comprising:

forming a semiconductor island over a substrate;

forming a gate electrode adjacent to the semiconductor island with a gate insulating film therebetween;

forming a source region, a drain region and a channel region formed between the source and drain regions,

wherein the first and second p-channel thin film transistors are connected in series,

wherein an off current from each of the first, second and third p-channel thin film transistors is less than [10-12] 10^{-12} A where a voltage of the drain region is 1V.

16. (Amended) A method according to claim [13] 15 further comprising [the step of]:

forming an interlayer insulating film including boro-phosphosilicate glass over the first, second and third p-channel thin film transistors and the n-channel thin film transistor.

17. (Amended) A method according to claim [13] 15, wherein the semiconductor island is a crystalline semiconductor island.

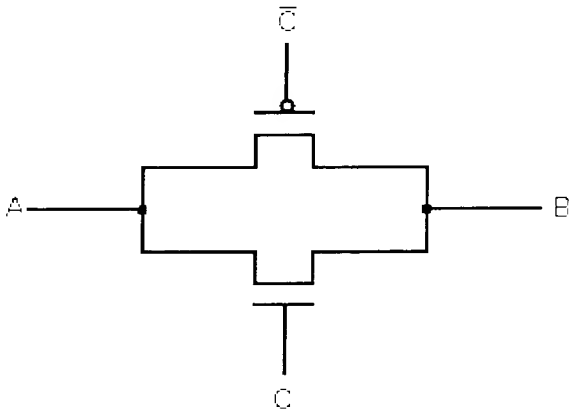
18. (Amended) A method according to claim [13] 15, wherein each of the source and drain regions of each of the first, second and third p-channel thin film transistors comprises boron.

19. (Amended) A method according to claim [13] 15, wherein each of the second source and drain regions of the n-channel thin film transistor comprises phosphorus.

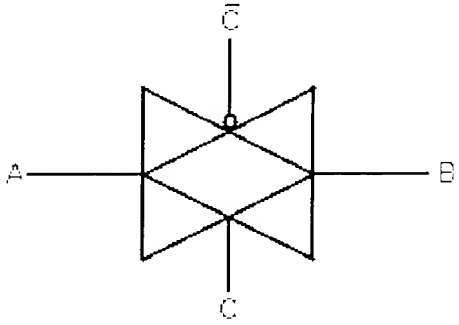
http://www.microlab.ch/courses/cbt/cbt-vlsi/trans_gate1.html

Transmission gate

The basic NMOS and PMOS transistors find ready application in switch-based logic arrangements. Used in this way they are referred to as pass transistors. The p-type is good at passing "1", and n-type is good at passing "0". By combining the n and p pass transistors in parallel we may produce a switch which faithfully transmits good logic "1" and good logic "0" levels. It is called transmission gate.



Such a gate is represented by a following symbol.



The table below shows how the transmission gate works.

C	result
0	A disconnected from B
1	A connected to B

http://users.ece.gatech.edu/~rdanse/ECE2030/slides/ECE2030_Chapter02_2pp.pdf

CHAPTER II

SWITCH NETWORKS AND SWITCH DESIGN

SWITCH NETWORKS

BASIC IDEAL SWITCH

- Simplest structure in a computing system is a switch

IDEAL SWITCH

- Path exists between INPUT and OUTPUT if Switch is CLOSED or ON
- Path does not exist between INPUT and OUTPUT if SWITCH is OPEN or OFF

SWITCH NETWORKS

SWITCHES IN SERIES

SWITCHES IN SERIES

Truth Table

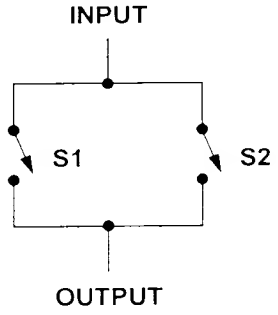
S1	S2	PATH?
OFF	OFF	NO
OFF	ON	NO
ON	OFF	NO
ON	ON	YES

- AND configuration

SWITCH NETWORKS

SWITCHES IN PARALLEL

SWITCHES IN PARALLEL



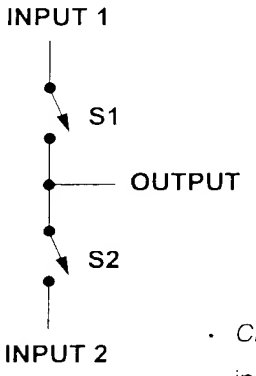
Truth Table

S1	S2	PATH?
OFF	OFF	NO
OFF	ON	YES
ON	OFF	YES
ON	ON	YES

- OR configuration

SWITCH NETWORKS

INPUT SELECTOR



Truth Table

S1	S2	OUTPUT
OFF	OFF	NONE
OFF	ON	INPUT 2
ON	OFF	INPUT 1
ON	ON	UNKNOWN

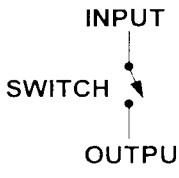
- *Crowbarred* level where logic level is indeterminate. Likely avoid this case.

CMOS

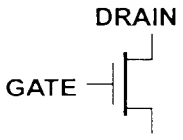
CMOS SWITCHES

- The idea is to use the series and parallel switch configurations to route signals in a desired fashion.
- Unfortunately, it is difficult to implement an ideal switch as given.
- Complementary Metal Oxide Semiconductor (CMOS) devices give us some interesting components.

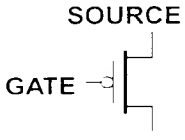
IDEAL SWITCH



nMOS transistor

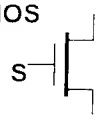


pMOS transistor



CMOS
TRANSFER CHARACTERISTICS

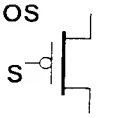
nMOS



S	SWITCH
0	OPEN
1	CLOSED

- nMOS when CLOSED
  - Transmits logic level 0 well
  - Transmits logic level 1 poorly

pMOS

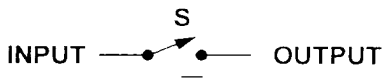


S	SWITCH
0	CLOSED
1	OPEN

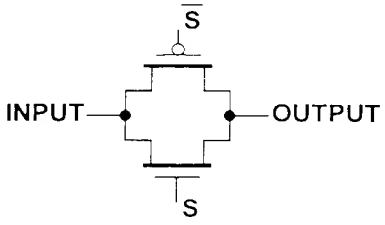
- pMOS when CLOSED
  - Transmits logic level 1 well
  - Transmits logic level 0 poorly

CMOS
TRANSMISSION GATE (1)

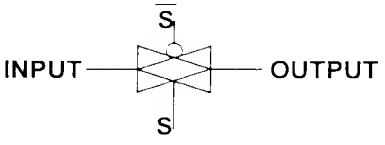
IDEAL SWITCH



CMOS TRANSMISSION GATE
(SWITCH)



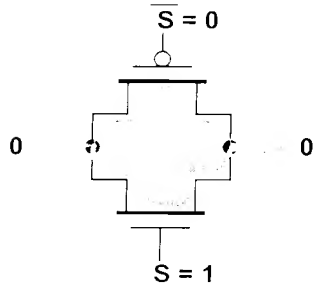
S	nMOS	pMOS	OUTPUT
0	OFF	OFF	Z
1	ON	ON	INPUT



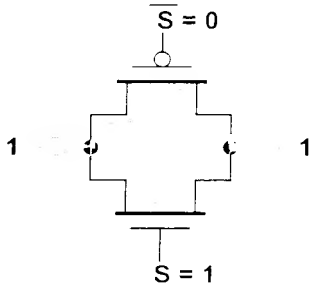
CMOS
TRANSMISSION GATE (2)

SPLIT OF CURRENT ACROSS A TRANSMISSION GATE FOR LOGIC-0 AND LOGIC-1 INPUT

LOGIC-0 AT INPUT



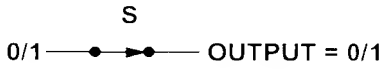
LOGIC-1 AT INPUT



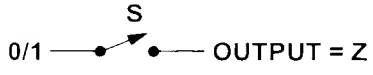
SWITCH NETWORKS
HIGH IMPEDANCE Z (1)

- With switches, we can consider three states for an output:
  - Logic-0
  - Logic-1
  - High Impedance **Z**

- Path exists for Logic-0 and Logic-1 when the switch is CLOSED.



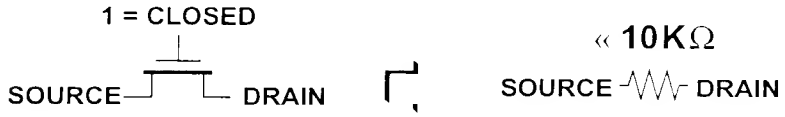
- High impedance is a state where the switch is OPEN.



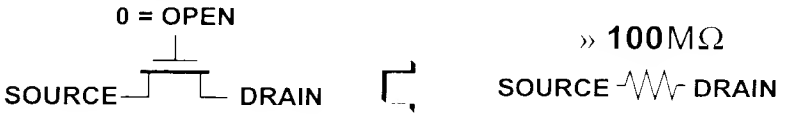
SWITCH NETWORKS

HIGH IMPEDANCE Z (2)

- Another way of thinking of switches is as follows
  - Path exists for Logic-0 and Logic-1 when the switch is CLOSED, meaning that the **impedance/resistance is small** enough to allow amply flow of current.



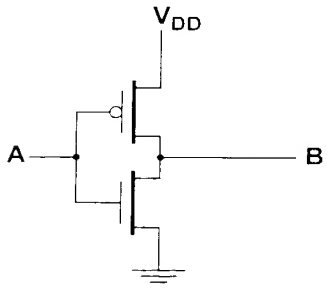
  - High impedance is a state where the switch is OPEN, meaning that the **impedance/resistance is very large** allowing nearly no current flow.



SWITCH NETWORKS

INVERTER (NOT)

$$B = \bar{A}$$



PULL-DOWN		PULL-UP			
A	B	A	B	A	B
0	Z	0	1	0	1
1	0	1	Z	1	0

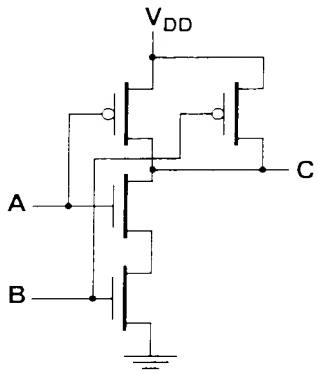
- This network inverts the binary input value.

SWITCH DESIGN
CHAPTER II-13
SWITCH DESIGN

SWITCH NETWORKS

NAND NETWORK

- CMOS
- SWITCH NETWORKS
  - -HIGH IMPEDANCE Z
  - -INVERTER



$$C = \overline{AB}$$

PULL-DOWN			PULL-UP		
A	B	C	A	B	C
0	0	Z	0	0	1
0	1	Z	0	1	1
1	0	Z	1	0	1
1	1	0	1	1	Z

→

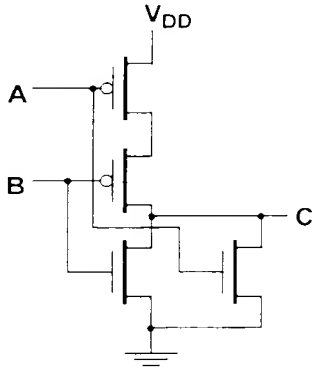
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

SWITCH DESIGN
CHAPTER II-14
SWITCH DESIGN

SWITCH NETWORKS

NOR NETWORK

- SWITCH NETWORKS
  - -HIGH IMPEDANCE Z
  - -INVERTER
  - -NAND NETWORK



$$C = \overline{A + B}$$

PULL-DOWN			PULL-UP		
A	B	C	A	B	C
0	0	Z	0	0	1
0	1	0	0	1	Z
1	0	0	1	0	Z
1	1	0	1	1	Z

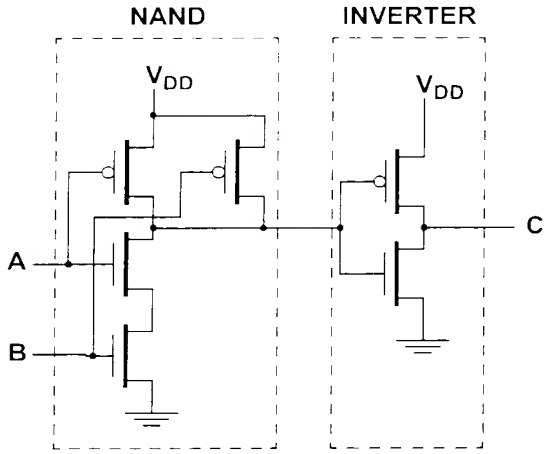
→

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

SWITCH DESIGN
CHAPTER II-15
SWITCH DESIGN

SWITCH NETWORKS
AND NETWORK

- SWITCH NETWORKS
  - -INVERTER
  - -NAND NETWORK
  - -NOR NETWORK



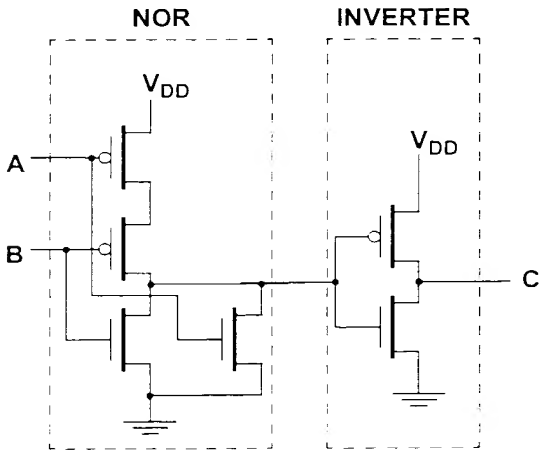
$$C = AB$$

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

SWITCH DESIGN
CHAPTER II-16
SWITCH DESIGN

SWITCH NETWORKS
OR NETWORK

- SWITCH NETWORKS
  - -NAND NETWORK
  - -NOR NETWORK
  - -AND NETWORK



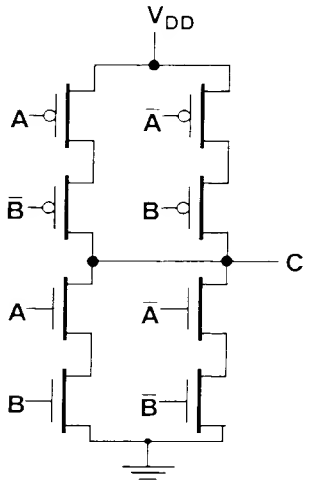
$$C = A + B$$

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

SWITCH NETWORKS

XOR NETWORK

- SWITCH NETWORKS
  - -NOR NETWORK
  - -AND NETWORK
  - -OR NETWORK



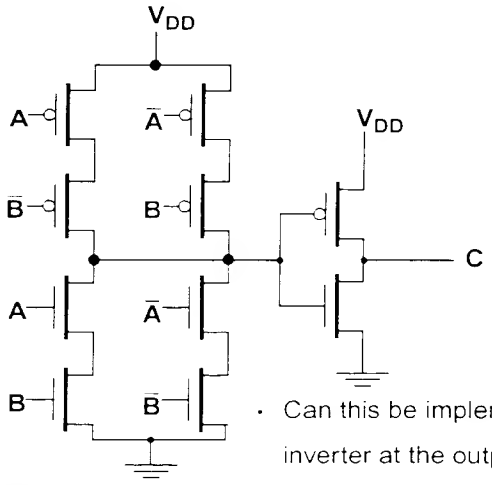
$$C = A\bar{B} + \bar{A}B$$

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

SWITCH NETWORKS

XNOR NETWORK

- SWITCH NETWORKS
  - -AND NETWORK
  - -OR NETWORK
  - -XOR NETWORK



$$C = \overline{A\bar{B} + \bar{A}B}$$

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

- Can this be implemented without the extra inverter at the output? Answer: Yes!

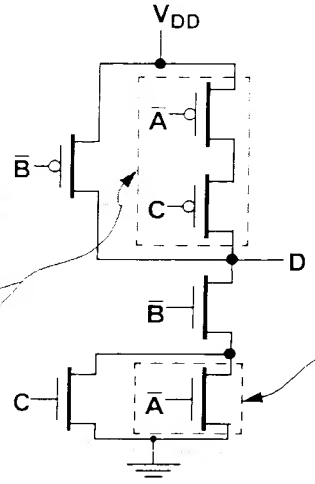
SWITCH NETWORKS

PULL-UP PULL-DOWN

$D = A\bar{C} + B$

PULL-UP

A	B	C	D
0	0	0	Z
0	0	1	Z
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	Z
1	1	0	1
1	1	1	1



PULL-DOWN

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	Z
0	1	1	Z
1	0	0	Z
1	0	1	0
1	1	0	Z
1	1	1	Z

SWITCH NETWORKS

FUNCTION IMPLEMENTATION

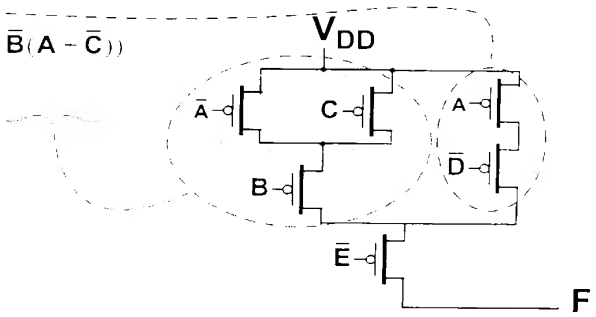
- Most Boolean functions can be easily implemented using switches.
- The basic rules are as follows
  - **Pull-up** section of switch network
    - **Use complements** for all literals in expression
    - Use only **pMOS devices**
    - Form **series** network for an **AND** operation
    - Form **parallel** network for an **OR** operation
  - **Pull-down** section of switch network
    - **Use complements** for all literals in expression
    - Use only **nMOS devices**
    - Form **parallel** network for an **AND** operation
    - Form **series** network for an **OR** operation

SWITCH NETWORKS

EXAMPLE PULL-UP

- To implement the Boolean function given below, the following pull-up network could be designed.

$$F = E(\bar{A}D + \bar{B}(A + \bar{C}))$$

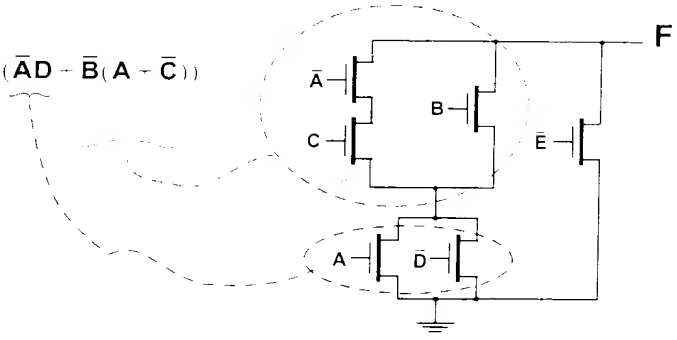


SWITCH NETWORKS

EXAMPLE PULL-DOWN

- To complete the switch design, the pull-down section for the Boolean function must also be designed.

$$F = E(\bar{A}D + \bar{B}(A + \bar{C}))$$



- Notice how **AND** and **OR** become **OR** and **AND** circuits, respectively.

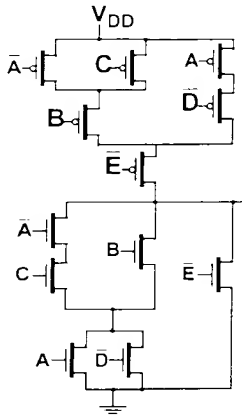
SWITCH NETWORKS

COMPLETED EXAMPLE

- Putting the pull-up and pull-down pieces together gives the following CMOS switch implementation of the Boolean function.

PULL-UP

PULL-DOWN



$$F = E(\bar{A}D + \bar{B}(A + \bar{C}))$$